SoC Performance Verification Using Transaction Level Model
Kevin Peregrine, Prashant Ravi, Lingyi Liu

Our Goal
- Better understand SystemC based Transaction level model to improve efficiency and verify System on a chip (SoC) designs

SystemC
- System level modeling language
- Alternative to VHDL and Verilog
- All coded in C++

TLM
- Transaction based modeling
- Extension to SystemC
- Allows for more abstraction

AMBA-PV Model
- CPU
- DMA
- AMBA-PV Bus
- Memory1
- Memory2