The image contains a digital logic diagram with waveforms for various signals. The signals include:

- clk
- reset
- W_addr
- W_data
- W_en
- R_addrA
- R_dataA
- R_addrB
- R_dataB

The diagram shows the timing of these signals over time. The values for W_data are 0xa, 0x1, 0x5, 0xf, and 0xe at certain times. The reset signal is active at the beginning, and the clk signal is active repeatedly.

The diagram also includes a shift register circuit with inputs D3, D2, D1, and D0, and outputs Q3, Q2, Q1, and Q0. There are also inputs labeled 'reset' and 'enable' for the shift register.