Stalls and flushes

- Last time, we discussed **data hazards** that can occur in pipelined CPUs if some instructions depend upon others that are still executing.  
  - Many hazards can be resolved by **forwarding** data from the pipeline registers, instead of waiting for the writeback stage.  
  - The pipeline continues running at full speed, with one instruction beginning on every clock cycle.

- Today we’ll see some real limitations of pipelining.  
  - Forwarding may not work for data hazards from load instructions.  
  - Branches affect the instruction fetch for the next clock cycle.

- In both of these cases we may need to slow down, or **stall**, the pipeline.
Data hazard review

- A data hazard arises if one instruction needs data that isn’t ready yet.
  - Below, the AND and OR both need to read register $2$.
  - But $2$ isn’t updated by SUB until the fifth clock cycle.
- Dependency arrows that point backwards indicate hazards.

```
Clock cycle
1   2   3   4   5   6   7

sub $2, $1, $3

and $12, $2, $5

or $13, $6, $2
```
Forwarding to the rescue!

- The desired value ($1 - $3) has actually already been computed—it just hasn’t been written to the registers yet.
- **Forwarding** allows other instructions to read ALU results directly from the pipeline registers, without going through the register file.

```
sub $2, $1, $3

and $12, $2, $5

or $13, $6, $2
```
What about loads?

- Imagine if the first instruction in the example was LW instead of SUB.
  - How does this change the data hazard?

```
lw  $2, 20($3)
and $12, $2, $5
```
What about loads?

- Imagine if the first instruction in the example was LW instead of SUB.
  - The load data doesn’t come from memory until the end of cycle 4.
  - But the AND needs that value at the beginning of the same cycle!
- This is a “true” data hazard—the data is not available when we need it.
Stalling

- The easiest solution is to **stall** the pipeline.
- We could delay the AND instruction by introducing a one-cycle delay into the pipeline, sometimes called a **bubble**.

```
lw  $2, 20($3)

and  $12, $2, $5
```

- Notice that we’re still using forwarding in cycle 5, to get data from the MEM/WB pipeline register to the ALU.
### Stalling and forwarding

- Without forwarding, we’d have to stall for *two cycles* to wait for the LW instruction’s writeback stage.

![Diagram showing execution pipeline](image)

```
lw $2, 20($3)
and $12, $2, $5
```

- In general, you can always stall to avoid hazards—but dependencies are very common in real code, and stalling often can reduce performance by a significant amount.
Stalling delays the entire pipeline

- If we delay the second instruction, we’ll have to delay the third one too.
  - Why? (two reasons)

```
lw $2, 20($3)
and $12, $2, $5
or $13, $12, $2
```
Stalling delays the entire pipeline

- If we delay the second instruction, we’ll have to delay the third one too.
  - This is necessary to make forwarding work between AND and OR.
  - It also prevents problems such as two instructions trying to write to the same register in the same cycle.

```
lw $2, 20($3)
and $12, $2, $5
or $13, $12, $2
```
Implementing stalls

- One way to implement a stall is to force the two instructions after LW to pause and remain in their ID and IF stages for one extra cycle.


- This is easily accomplished.
  - Don’t update the PC, so the current IF stage is repeated.
  - Don’t update the IF/ID register, so the ID stage is also repeated.

```plaintext
lw  $2, 20($3)
and $12, $2, $5
or  $13, $12, $2
```
But what about the ALU during cycle 4, the data memory in cycle 5, and the register file write in cycle 6?

Those units aren’t used in those cycles because of the stall, so we can set the EX, MEM and WB control signals to all 0s.
The effect of a load stall is to insert an empty or **nop** ("no operation") instruction into the pipeline.
Detecting stalls

- Detecting stall is much like detecting data hazards.

- Recall the format of hazard detection equations:

  ```plaintext
  if (EX/MEM.RegWrite = 1
      and EX/MEM.RegisterRd = ID/EX.RegisterRd)
  then Bypass Rs from EX/MEM stage latch
  ```

  sub $2, $1, $3

  and $12, $2, $5
Detecting Stalls, cont.

- When should **stalls** be detected?

  \[
  \text{lw} \quad \$2, \ 20(\$3) \quad \text{and} \quad \$12, \ $2, \ $5
  \]

- What is the stall condition?

  \[
  \text{if (}
  \]

  \[
  \text{then stall}
  \]

  \[
  \text{)}
  \]
Detecting stalls

- We can detect a load hazard between the current instruction in its ID stage and the previous instruction in the EX stage just like we detected data hazards.
- A hazard occurs if the previous instruction was LW...

\[ ID/EX.\text{MemRead} = 1 \]

...and the LW destination is one of the current source registers.

\[ ID/EX.\text{RegisterRt} = IF/ID.\text{RegisterRs} \]
\[ \text{or} \]
\[ ID/EX.\text{RegisterRt} = IF/ID.\text{RegisterRt} \]

- The complete test for stalling is the conjunction of these two conditions.

\[
\text{if } (ID/EX.\text{MemRead} = 1 \text{ and} \\
(ID/EX.\text{RegisterRt} = IF/ID.\text{RegisterRs} \text{ or} \\
ID/EX.\text{RegisterRt} = IF/ID.\text{RegisterRt})) \text{ then stall}
\]
Adding hazard detection to the CPU
Adding hazard detection to the CPU
The hazard detection unit

- The hazard detection unit’s inputs are as follows.
  - `IF/ID.RegisterRs` and `IF/ID.RegisterRt`, the source registers for the current instruction.
  - `ID/EX.MemRead` and `ID/EX.RegisterRt`, to determine if the previous instruction is LW and, if so, which register it will write to.

- By inspecting these values, the detection unit generates three outputs.
  - Two new control signals `PCWrite` and `IF/ID Write`, which determine whether the pipeline stalls or continues.
  - A **mux select** for a new multiplexer, which forces control signals for the current EX and future MEM/WB stages to 0 in case of a stall.
Generalizing Forwarding/Stalling

- What if data memory access was so slow, we wanted to pipeline it over 2 cycles?

- How many bypass inputs would the muxes in EXE have?
- Which instructions in the following require stalling and/or bypassing?

<table>
<thead>
<tr>
<th>Clock cycle</th>
<th>IM</th>
<th>Reg</th>
<th>DM</th>
<th>Reg</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IM</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>Reg</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td>DM</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

lw          r13, 0(r11)
addd          r7, r8, r9
add          r15, r7, r13
Branches in the original pipelined datapath

When are they resolved?

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Stalls and flushes

Branches in the original pipelined datapath

When are they resolved?
Branches

- Most of the work for a branch computation is done in the EX stage.
  - The branch target address is computed.
  - The source registers are compared by the ALU, and the Zero flag is set or cleared accordingly.
- Thus, the branch decision cannot be made until the end of the EX stage.
  - But we need to know which instruction to fetch next, in order to keep the pipeline running!
  - This leads to what’s called a **control hazard**.

```
beq $2, $3, Label
```

<table>
<thead>
<tr>
<th>Clock cycle</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>IM</td>
<td>Reg</td>
<td>IM</td>
<td>DM</td>
<td>Reg</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

???

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Stalls and flushes
Stalling is one solution

- Again, stalling is always one possible solution.

- Here we just stall until cycle 4, after we do make the branch decision.
Another approach is to guess whether or not the branch is taken.
- In terms of hardware, it’s easy to just assume the branch is not taken.
- This way we just increment the PC and continue execution, as for normal instructions.

If we’re correct, then there is no problem and the pipeline keeps going at full speed.

```
+-----+-----+-----+-----+-----+-----+-----+
| IM  | Reg | IM  | Reg | IM  | DM  | Reg |
+-----+-----+-----+-----+-----+-----+-----+
beq $2, $3, Label
   next instruction 1
   next instruction 2
```

Clock cycle

1  2  3  4  5  6  7
Branch misprediction

- If our guess is wrong, then we would have already started executing two instructions incorrectly. We’ll have to discard, or flush, those instructions and begin executing the right ones from the branch target address, Label.

```
beq $2, $3, Label
```

next instruction 1

next instruction 2

Label: . . .
Performance gains and losses

- Overall, branch prediction is worth it.
  - Mispredicting a branch means that two clock cycles are wasted.
  - But if our predictions are even just occasionally correct, then this is preferable to stalling and wasting two cycles for every branch.

- All modern CPUs use branch prediction.
  - Accurate predictions are important for optimal performance.
  - Most CPUs predict branches dynamically—statistics are kept at run-time to determine the likelihood of a branch being taken.

- The pipeline structure also has a big impact on branch prediction.
  - A longer pipeline may require more instructions to be flushed for a misprediction, resulting in more wasted time and lower performance.
  - We must also be careful that instructions do not modify registers or memory before they get flushed.
Implementing flushes

- A flush is required when the instruction in EX is a BEQ and “zero” is 1.
- This flush introduces two bubbles into the pipeline:
  - Like the load stalls, we need to nop the instruction in the ID stage.
  - We can flush an instruction from the IF stage by replacing it in the IF/ID pipeline register with a harmless nop instruction.
    - MIPS uses `sll $0, $0, 0` as the nop instruction.
    - This happens to have a binary encoding of all 0s: 0000 .... 0000.
- The IF.Flush control signal shown on the next page implements this idea.
Branches in the original pipelined datapath

When are they resolved?

Instruction memory

Read Instruction address [31-0]

PC Src

Add

RegWrite

Control

IF/ID

ID/EX

EX/MEM

MEM/WB

MemWrite

MemToReg

Data memory

Address

Write data

Read data

IF.Flush

Instr [15 - 0]

Instr [15 - 11]

Instr [20 - 16]

Write register

Write data

Instr [31-0]

Read address

Instruction

Read data 1

Read data 2

Write register

Write data

Sign extend

RegDst

RegWrite

RegDst

Shift left 2

ALU Zero

Result

ALUSrc

ALUOp

Add

Add

MemRead

MemWrite

M

M

M

M

WB

WB

WB

WB

When are they resolved?

Stall || IF.Flush

IF.Flush

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Summary

- Three kinds of hazards conspire to make pipelining difficult.
  - **Structural hazards** result from not having enough hardware available to execute multiple instructions simultaneously.
    - These are avoided by adding more functional units (e.g., more adders or memories) or by redesigning the pipeline stages.
  - **Data hazards** can occur when instructions need to access registers that haven’t been updated yet.
    - Hazards from R-type instructions can be avoided with forwarding.
    - Loads can result in a “true” hazard, which must stall the pipeline.
  - **Control hazards** arise when the CPU cannot determine which instruction to fetch next.
    - We can minimize delays by doing branch tests earlier in the pipeline.
    - We can also take a chance and predict the branch direction, to make the most of a bad situation.