DESIGN OF THE LC-3 DATA PATH

Data path control signals
There are a total of 49 control signals, but for now we will focus on 25 of those signals.
* Load signals:
If LD.X=1, load register X
If LD.X=0, don’t load register X

Set all signals to 0 except for those that need to be loaded
* Gate signals:
If Gate $X=1$, put value in register $X$ in global bus

If Gate $X=0$, set tri-state buffer to high-impedance

Never allow more than one Gate $X$ value to be $1
* MUX signals:
Select input

If the output of the MUX is not used, then select lines can be don't care
Memory signals:
If M10.EN=1 then memory is enabled to read (R.W=0) or write (R.W=1)
If M10.EN=0 then memory is disabled and R.W can be don't care
* ALU

ALUK selects either

ADD

AND

NOT A

PASS A

If output of ALU is not used, then we can set ALUK to don’t care
Instruction cycle

Question:
How do you set control signals to implement each phase in the instruction cycle?
* State 18:

$$\text{MAR} \leftarrow \text{PC}$$

$$\text{PC} \leftarrow \text{PC} + 1$$
* State 33:
State 32:
* State 1 (ADD):