Other bit-sliced design

1. Compare 2 unsigned integers
2. Logical Unit

1. Comparator

   ① \( x = 0 \) \( \bar{y} = 0 \) \( x_0 \neq y_0 \)
   \( x > y \)
   \( x_0 > y_0 \)
   \( x < y \)

   ② \( x = 1 \) \( \bar{y} = 1 \)
   \( (i) \ x_0 = y_0 \)
   \( (ii) \ x_1 > y_1 \)

Outcome of lower order bits does not impact the outcome
Outcome of lower order bits does impact the outcome of the higher order bits.

\[ x \begin{array}{c} 0 \ 0 \end{array} \]
\[ y \begin{array}{c} 0 \ 1 \end{array} \]

\( (i) \ x_0 < y_0, \ x < y \)
\( (ii) \ x_i = y_i \)

Outcome of lower order bits does impact the outcome of the higher order bits.

\[ x \begin{array}{c} 0 \ 1 \end{array} \]
\[ y \begin{array}{c} 0 \ 0 \end{array} \]

Taken together we need a bit-slice comparison AND need information of comparison of lower-order bits.

Abstract Model:
Abstract Model:

1. **Need:**
   - \( a_i > b_i \)
   - \( a_i < b_i \)
   - \( a_i = b_i \)

2. **Inputs:** \( a_i, b_i \), result of comparison from previous bit-slice.

Truth table:

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inputs</td>
<td>Outputs</td>
<td>Representation</td>
</tr>
<tr>
<td>--------</td>
<td>---------</td>
<td>----------------</td>
</tr>
<tr>
<td>(a_i) (b_i) (C_1) (C_0)</td>
<td>(Z_0) (Z_1)</td>
<td>(C_1) (C_0)</td>
</tr>
<tr>
<td>0 0 0 0</td>
<td>0 0</td>
<td>0 0</td>
</tr>
<tr>
<td>0 0 0 1</td>
<td>0 1</td>
<td>0 1</td>
</tr>
<tr>
<td>0 0 1 0</td>
<td>1 0</td>
<td>1 0</td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>1 X</td>
<td>1 X</td>
</tr>
</tbody>
</table>
\begin{align*}
\begin{array}{cccc}
00 & 01 & 11 & 10 \\
\begin{array}{c}
0 \\
1 \\
\end{array} & \begin{array}{c}
1 \\
1 \\
\end{array} & \begin{array}{c}
X \\
X \\
\end{array} & \begin{array}{c}
0 \\
1 \\
\end{array} \\
\end{array}
\end{align*}
\[ z_1 = a_i b_i' + a_i c_i + b_i c_i \]
\[ z_0 = b_i c_0 + a_i c_0 + a_i b_i \]
Comparing 2's complement integers: 2.4.5 Prof. Lumetta notes.

**Logical Unit**

**Bitwise Operation**

<table>
<thead>
<tr>
<th>Functions</th>
<th>Control bits $k_1k_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_1$</td>
<td>A AND B</td>
</tr>
<tr>
<td>$f_2$</td>
<td>A OR B</td>
</tr>
<tr>
<td>$f_3$</td>
<td>A NAND B</td>
</tr>
<tr>
<td>$f_4$</td>
<td>0</td>
</tr>
</tbody>
</table>

$k_1k_0$
\[ L \ (SOP) = a_i b_i k'_i + b_i k'_i k_0 + a_i k'_i k_0' + a_i' k'_i k_0' + b_i' k_i k_0' \]