Announcement

Suppose we don't wish to only store, need to control the bit that is stored. Need to change $Q$ as needed.

1. How do we make $Q=1$ (set $Q$)

Consider input $\overline{S}$ (active low) does its activity (setting $Q=1$) when $S=0$.

<table>
<thead>
<tr>
<th>$Q$</th>
<th>$P$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Circuit stores a bit.
when $S=0$

<table>
<thead>
<tr>
<th>$\overline{S}$</th>
<th>Q</th>
<th>P</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Set $Q$

\[
\begin{array}{c|c|c}
\overline{S} & Q & P \\
0 & 0 & 1 \\
1 & 1 & 0 \\
\end{array}
\]

\[
\overline{S}
\]

\[
\text{Q}
\]

\[
\text{P}
\]

(i) When $\overline{S} = 1$, ANDing any value with 1 produces same value

(ii) When $\overline{S} = 0$,

- Upper gate output forced to 1
- Lower gate output forced to 0

\[
\therefore Q \text{ is set}
\]

\[
\times \cdot 1 = \times
\]
2) How do we make $Q=0$? (Reset)

<table>
<thead>
<tr>
<th>$\overline{R}$</th>
<th>$\overline{S}$</th>
<th>$Q$</th>
<th>$P$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
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<td>1</td>
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</tbody>
</table>

$\overline{S} \overline{R}$ latch

$S' \overline{R}' = 0 \overline{0}$  $Q = 1$, $P = 1$
$S = 1$, $P = 1$
$\overline{R} \overline{S} = 11$  $Q = 0$

Symbol

Undesirable

How do we avoid $\overline{S} \overline{R} = 00$
Now we have
\[
\overline{S} \overline{R} \text{ latch}
\]

\[
\overline{D} \text{ latch}
\]

This ensures \( \overline{SR} = 00 \) will not happen, but cannot hold a bit!

Solution: Gated D-latch.
Gated D-latch

\[
\begin{array}{llllll}
& & & & & \\
& & & & & \\
& & & & & \\
& & & & & \\
& & & & & \\
& & & & & \\
& & & & & \\
\end{array}
\]

Obs:
(i) \( WE = 1 \quad Q = D \); \( WE = 0 \), \( Q \) holds
(ii) \( P = Q' \)

Symbol: Gated D-latch

\[
\begin{array}{llllll}
WE & D & Q & Q' \\
\end{array}
\]
Problem: If \( WE = 1 \), and \( D \) keeps changing, \( Q \) changes as a result (an undesirable property). This is because we want to have "an output" that can be used by other circuits that rely on \( Q \). To achieve this, allow change to happen only at a specific instance (thus giving other cKts. to use the output).

Solution: Allow state change to happen only at "an edge", say when \( WE \) goes 0 to 1 (or 1 to 0).
when WE goes 0 to 1 (or 1 to 0).

D Flip-flop

Operation: Some value of Q is available when all are low. Latch 1 gets WE=1, latch 2 gets WE=0.
Operation: Some value of $x$ is available.
* When $clk$ is low, latch 1 gets $WE=1$, latch 2 gets $WE=0$.
  Result: $D$ is copied to $x$, latch 2 holds $Q$.
* When $clk$ is high, latch 1 gets $WE=0$, latch 2 gets $WE=1$.
  Result: latch 1 holds $x$, latch 2 copies $x$ to $Q$.

CLK=0, $x=D$, $Q$ holds
CLK=1, $x$ holds, $Q=x$. 
Effect: $D$ is copied to $Q$ when clock goes from low to hi. (positive edge)

$\text{Symbol:}$ Positive edge triggered $D$ FF  $\begin{array}{c} \downarrow \\
D \quad Q
\end{array}$
Positive edge triggered D FF

Negative edge triggered D FF