Lecture 25: Memory

Gated D-latch, FF, RS latch

Memory is a group of storage elements and necessary logic to move data into & out of it.
Abstract Memory model:
6 × 8 bit memory
6 Byte memory

Address space

Addressability

2^k Address space
Interface

Read/Write
Chip Select

RAM cell

Select = 0
= 1

not operational
operational

2^k \times N RAM

DATA
ADDRESS
R/W'
CS

N

Data out

B

C
Increase addressability

Increase address space?
1 MB RAM

How many address lines?

1 MB $\rightarrow (1024)^2 \times 8$ bits

$\left(\frac{10^6}{2}\right)^2 \times 8$ bits
20 address lines

2 x 8 bit RAM
Build larger memory from smaller units

Build a 32 x 8 RAM using a 1:2 decoder and 2 16 x 8 RAMs
units

and
DATA_IN
A[4:0]
DATA IN
ADDRS
CS
R/W

1:2 decoder
E
I
0
1

DATA 16x8
ADDRS
CS
R/W
OUT

DATA 16x8
ADDRS
CS
R/W
OUT

32x8
RAM

x8
M
V

x8
M
V

OUT