LC-3 INSTRUCTION SET ARCHITECTURE

The LC-3 datapath
Global bus:
16 wires and associated electronics, bidirectional bus
Memory:
Accessed by loading address in MAR, data to be read/written is loaded in MDR
Register file:
Consists of eight 16-bit registers

ALU:
Processing element
PC:
Supplies to MAR address of instruction to be fetched

PCMUX:
Supplies address to PC depending on instruction being executed
MARMUX: Controls which source will supply address to MAR
LC-3 instruction cycle and FSM
ISA specifies all information about the computer that the software has to be aware of.

1) Memory organization:
   16-bit addressability, $2^{16}$ address space

2) Registers:
   Eight General Purpose Registers (GPR) R0–R7,
   16 bits per register
3) Data types:
   Types of information representation the ISA can operate on

   LC-3 only handles 16-bit 2's complement integers

4) Addressing modes:
   Mechanism for specifying where operands are located

   Operands can be located in: memory, register, part of instruction

   Memory modes: PC-relative, indirect, base+offset
5) Condition codes:
Allow instruction sequencing to change based on previous result.

LC-3 has three single-bit registers that are set or cleared when a 6PR is written:

N: negative result
Z: zero result
P: positive result
6) Instruction set:

Operate

Data movement

Control