MEMORY

So far
* S-R latch
* D latch
* D flip-flop
* Registers

Today
Memory: group of storage elements and necessary logic to move data in & out
Memory model

Let's consider a memory with 4 locations, each storing 8 bits of information:

```
  0010 1101
  1010 0000
  1111 0101
  0011 1100
```
Interface

Data In $\rightarrow^n DATA$
Address $\rightarrow^K ADDRS$
Chip Select $\rightarrow CS$
Read/Write $\rightarrow R/W$

$Z^k \times n$ RAM

OUT $\rightarrow^n Data Out$

Question: is memory synchronous or asynchronous?
RAM cell

Implementation:

SELECT

B

C

\overline{B}

\overline{C}
Model:
**Symbol:**

```
S
```

```
RAM CELL
```

```
B
```

```
C
```

**Question:** How do we increase the address space?
Bit slice

Memory capable of storing $M$ 1-bit values

Question: how can I get larger addressability?
Multibit memory

Word select 0

Word select 1

Question: how many word select lines do we have for a $2^{20} \times 8$ RAM (1 MB)?
Decoders & memories
Building larger memories

Example: build a 32Kx8 RAM from two 16Kx8 RAM modules and a 1:2 decoder