FSM DESIGN EXAMPLES

Fixing alarm duration

Previously, we studied an FSM for a keyless car entry system:

Inputs (buttons):

Outputs:
The implementation would be similar to this:

![Diagram with state machines and logic gates]

Question: how do we turn off the alarm after some period of time?

We need to replace ALARM state for countdown states:

- ALARM T-1
- ALARM T-2
- ALARM 0
Question: is there an alternative way?

Let's assume we have access to a count down counter with parallel load functionality:

![Diagram of a counter with parallel load]

Question: when should we make LD=1?

Answer: when panic button is pressed (P=1)
Question: how do we move to the LOCKED state when timeout occurs?

Hint: we need to transition from ALARM (originally 01) to LOCKED (originally 00)

Solution: force $S_0 = 0$ when we are in ALARM state ($S_1, S_0 = 01$), panic button has not been pressed ($P = 0$) and counter has timed out ($Z = 1$)

\[
F = \begin{cases} 
1 & \text{(force } S_0 = 0) \\
0 & \text{(hold } S_0) 
\end{cases}
\]
Final circuit: