MEMORY

So far
* S-R latch
* D latch
* D flip-flop
* Registers

Today
Memory: group of storage elements and necessary logic to move data in & out
Let's consider a memory with 4 locations, each storing 8 bits of information:

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
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</thead>
<tbody>
<tr>
<td>0010</td>
<td>1101</td>
<td></td>
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<tr>
<td>1010</td>
<td>0000</td>
<td></td>
<td></td>
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<tr>
<td>1111</td>
<td>0101</td>
<td></td>
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<tr>
<td>0011</td>
<td>1100</td>
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</tbody>
</table>
Interface

Data In $n \rightarrow$ DATA
Address $K \rightarrow$ ADDRS
Chip Select $\rightarrow$ CS
Read/Write $\rightarrow$ R/W

$\triangleleft$ OUT $\rightarrow n \rightarrow$ Data Out

$\mathbb{Z}^K \times n$ RAM
RAM cell

Implementation:

\[
\begin{array}{c}
\text{SELECT} \\
\text{B} \\
\text{Q} \\
\text{Q'} \\
\text{B'} \\
\text{C}
\end{array}
\]
Symbol:

RAM CELL

Question: how do we increase the address space?
Bit slice

Memory capable of storing $M$ 1-bit values

Question: how can I get larger addressability?
Multibit memory

Word select 0

B RAM CELL C
B

Word select 1

B RAM CELL C
B

Question: how many word select lines do we have for a $2^{20} \times 8$ RAM (1 MB)?
Decoders & memories

2:4 decoder

ADDRS1
S1

ADDRS0
S0

0
1
2
3

RAM CELL
B

RAM CELL
B

RAM CELL
B

RAM CELL
B

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Building larger memories

Example: build a 32 K x 8 RAM from two 16 K x 8 RAM modules and a 1:2 decoder

32 K x 8 RAM

1:2 decoder
E 0
I 1

DATA
ADDRS
CS
R/W

OUT

DATA
ADDRS
CS
R/W

OUT