CS 296-33: Intro to Xilinx Vivado

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FPGA Design Flow
Basys3

- 1,800 Kbits of fast block RAM
- 33,280 logic cells in 5200 slices (each slice contains four 6-input LUTs and 8 flip-flops)
- Five clock management tiles, each with a phase-locked loop (PLL)
- 90 DSP slices
- Internal clock speeds exceeding 450MHz
- On-chip analog-to-digital converter (XADC)
- 16 User Switches
- 16 User LEDs
- 5 User Pushbuttons
- 4-digit 7-segment display
- Three Pmod connectors
- Pmod for XADC signals
- 12-bit VGA output
- USB-UART Bridge
- Serial Flash
- Digilent USB-JTAG port for FPGA programming and communication
- USB HID Host for mice, keyboards and memory sticks
Design Steps

• Step 1: Create a Project and add Verilog Modules
• Step 2: Simulate RTL
• Step 3: Synthesize
  • Generate Netlist
• Step 4: Implement
  • Translate
  • Map
  • Place and Route
• Step 5: Timing Simulation
• Step 6: Generate Bitstream and Program FPGA
What is Synthesis?

• Generates a Netlist from your design
• What is a Netlist?
  • Ports
  • Cells, or Design objects (gates, buffers, flip flops, etc…)
  • Nets (Wires)
• Basically draws out the logic circuit from your HDL
What now?

- Need to define a “Constraints file” (.xdc in Vivado)
  - Maps FPGA pins to Input and Outputs
  - Sets required timing constraints
- Once that is done, Implement Design
What is Implementing?

• Translate
  • Combines Netlist and Constraints File and translates to a Xilinx specific language

• Map
  • Maps the design onto FPGA elements (LUTs, Buffers, Flip-flops, etc…)

• Place and Route
  • Desides which actual (physical) resources of the FPGA to use and routes the wiring between them
What we are Designing?
For Your Information!

• You can either work in pairs or individually.
• Read the First page of the Handout (Not the Manual) carefully before you do anything.
• Create a folder called “images” under FPGALab0 in your svn directory
  • mkdir images
• Put all the screenshots in the images folder and commit them to svn
  • svn add images/
  • svn commit –m “commiting FPGA Lab 0”
• Do NOT program the board without the assistance of the instructor/TA.