Build a 2-input Multiplexor

Complete the code for a 2-input multiplexor below

```verilog
// output = A (when control == 0) or B (when control == 1)
module mux2(out, A, B, control); // a 2-input multiplexor
    output out;
    input A, B;
    input control;
endmodule // mux2
```

Draw the logic circuit for mux implemented above
New Verilog syntax

How would the verilog code above change if our inputs were 5 bit wide?

How is a half adder different from a full adder?
Let’s add adders

Complete the code for half adders and full adders below

```verilog
module half_adder(C, S, X, Y);  // a 1-bit half adder
  output  C, S;
  input   X, Y;
endmodule  // half_adder

module full_adder(Cout, S, X, Y, Cin);  // a 1-bit full adder
  output  Cout, S;
  input   X, Y, Cin;
endmodule  // full adder
```