Finite state machine design

You’ve been hired by a big technical company GoogBook to build a shredder that shreds every resume with a GPA below 4.0 and shreds every alternate resume with a 4.0 GPA.

To implement this, design a finite-state machine with a 1-bit input, $\text{perfectgpa}$, and a 1-bit output, $\text{shred}$, which is 1 when the input resume should be shredded.
Continuing FSM Design

- How many bits do we need to represent all states for the FSM above?

- Draw the sequential circuit for the FSM above.
Verilog is back

Complete the verilog code for the FSM described above.

```verilog
module shredder(done, shred, perfectgpa, clock, reset);
  output    done, shred;
  input     perfectgpa, reset;

  wire      sGarbage_next, sGarbage;

  sGarbage_next = reset;

  dffe fsGarbage(sGarbage, sGarbage_next, clock,
                 1'b1 /*enable*/, 1'b0 /*reset*/);

endmodule // shredder
```