Control Voltage Interface for SHARC Controller
Miguel Torres
Fall 2018
ECE 395: Advanced Digital Projects Lab
University of Illinois at Urbana-Champaign
Abstract

This module is an external peripheral interface for the Analog Devices SHARC processor. This design facilitates communication between modular synthesizer systems, through the use of Control Voltage (CV), and the I²C protocol for the SHARC processor. The PCB is specifically designed to comply with the Eurorack standard to easily integrate into existing modular systems. We attempted to make the design compatible with commonly used CV voltage ranges through the use of a gain reduction and offset circuit. However, due to calculations resulting in values of negative resistance, this circuit linearly maps the 5 Vpp range of voltages to a 0 V to 4 V range instead of a 0 V to 3.3 V range as originally expected. Barring the voltage mapping, this module is capable of providing 12-bit resolution at sampling frequencies of 50 kHz to 200 kHz, resulting in high precision of digitization for small changes in input voltage.
# Table of Contents

**Terms and Keywords**  
4

**Synthesizers**  
5

- What is a Synthesizer?  
5
- Modular Synthesizers  
5
- The Eurorack Standard  
5
- Control Voltage  
5

**Analog Devices SHARC Processor**  
6

- I2C  
6
- SPI  
6

**SHARC Peripheral Module**  
7

- Signal Flow Diagram  
7
- 4:1 Mux  
7
- Gain Reduction and Offset  
8
- ADC  
9
- I2C to SPI Bridge  
9

**Circuit Schematic**  
10

**Future Work**  
11

**References**  
12
Terms and Keywords

- ADC – Analog-to-Digital Converter
- CV – Control Voltage
- DC – Direct Current
- DIY – Do-It-Yourself
- DSP – Digital Signal Processing
- EG – Envelope Generator
- HP – Horizontal Pitch
- I²C – Inter-Integrated Circuit
- LFO – Low Frequency Oscillator
- MISO – Master Input Slave Output
- MOSI – Master Output Slave Input
- Mux – Multiplexer
- PCB – Printed Circuit Board
- SPI – Serial Peripheral Interface
- SPICE – Simulation Program with Integrated Circuit Emphasis
- SHARC – Super Harvard Architecture
- TWI – Two-Wire Interface
- U – Rack Unit
- VCA – Voltage-Controlled Amplifier
- VCO – Voltage-Controlled Oscillator
- Vpp – Volts peak-to-peak
Synthesizers

What is a Synthesizer?

Synthesizers, or synths for short, are electronic musical instruments. At the most basic level, a synthesizer is comprised of an electrical sound generator (oscillators or noise generators) whose amplitude, frequency, and sonic characteristics can be controlled by a user interface – most commonly a musical keyboard and potentiometers.

Modular Synthesizers

Early synthesizers were large complex units. In the 1960’s a modular approach to synthesizer building was popularized by Robert Moog and Donald Buchla – the pioneers of East Coast and West Coast synthesis, respectively. They focused on building systems comprising of interchangeable modules. Common modules found in most systems are: Voltage-Controlled Oscillators (VCO) – the sound generators, Voltage-Controlled Amplifiers (VCA) – which manage the amplitude of the VCO’s signal, Voltage-Controlled Filters (VCF) – which affect the frequency spectrum of the signal, and Envelope Generators (EG) – which shape the signal to have a specified transient shape. Other modules include Low Frequency Oscillators (LFO), CV/Gate Sequencers, and the list goes on. This method of building systems from modules caught on quite quickly and thus the Modular Synthesizer became the standard for synth systems.

The Eurorack Standard

Customizable modular synthesizers, popular in the 1970’s, are experiencing a come back. One of the leading manufacturing companies of modular synth systems is Doepfer Musikelektronik. Their Eurorack design is the unofficial standard for modular systems. This standard makes use of the rack mounting model of PCB enclosures used for digital systems. The Eurorack standard adheres to a 3 Rack Unit (3U) vertical dimension – where 1U is 44.45 mm (1.75 in) – and a module dependant horizontal dimension known as Horizontal Pitch (HP) – where 1 HP is 5.08 mm (0.20 in) – that can vary between 4 and 50 HP.

Control Voltage

Communication between modules is accomplished by a Direct Current (DC) signal known as Control Voltage (CV). The voltage range used is module and manufacturer specific. However, all manufacturers have adopted the 1 volt per octave model introduced by Robert Moog for determining pitch. Additionally, with Doepfer being a heavy influence on the Do-It-Yourself (DIY) modular synth community, a 5 volt peak-to-peak (Vpp) model is commonly used today; this can vary between -5 V to 0 V, -2.5 V to 2.5 V, or 0 V to 5 V.
Analog Devices SHARC Processor

The Analog Devices ADSP-21489 is one of the fourth generation processors of their SHARC family. The SHARC line of processors are based on a Super Harvard Architecture for floating-point processing. These processors are designed for high quality Digital Signal Processing (DSP) suitable for many applications. SHARC processors are compatible with SPI and two-wire interface (TWI) to interact with other devices.

I²C

The Inter-Integrated Circuit (I²C) protocol is a two-wire synchronous, serial interface that facilitates communication between low speed peripherals and their control systems. One thing to note, while I²C is a type of two-wire interface, it is not the same as TWI, however, I²C is mostly compatible with TWI. I²C uses Serial Clock (SCL) and Serial Data (SDA) signals on two bidirectional wires, requiring only the use of two pins for each device. The protocol allows for systems with multiple slave and master devices.

SPI

The Serial Peripheral Interface (SPI) protocol is a synchronous, serial protocol that commonly uses a 4-wire interface. Signals used in the protocol are the Serial Clock (SCLK), Master-Input Slave-Output (MISO), Master-Output Slave-Input (MOSI), and Slave Select (SS). This protocol can allow for multiple slaves – requiring additional pin connections from the master for each additional peripheral – but is most commonly configured for one master to one slave.
SHARC Peripheral Module

Signal Flow Diagram

Figure 1: Signal path for the SHARC peripheral module.

**4:1 Mux**

In order to prepare the CV signals for digitization, a 4 input to 1 output Multiplexor (Mux) is used to serialize the CV signals. This Mux cycles through each input, as controlled by the I^2C to SPI Bridge, passing the corresponding input’s signal through for further processing. In order to be able to pass a wide range of voltages while accepting 3.3 V Select signals, a dual supply Mux is required. Thus, Analog Device’s ADG509A 4:1 Mux was chosen. This Mux will handle up to ±12 V of analog signal, as determined by the input voltage powering the module, and 3.3 V digital high for the select inputs.
Gain Reduction and Offset

The serialized CV signal’s voltage range needs to be reduced from 5 Vpp to a range within 0 V to 3.3 V. Adding an offset while reducing the voltage range down to a maximum of 3.3 V, is accomplished with a linear mapping of input to output signals: $V_{out} = mV_{in} + b$, where $m$ represents the gain reduction and $b$ represents the offset. An Operational Amplifier, or op-amp for short is used to execute this linear mapping. Using a Non-Inverting configuration for the op-amp (see Figure 2) will realize the gain and offset needed.

\[
\begin{align*}
V_{o} & = mV_{u} + b \\
\end{align*}
\]

Figure 2: Schematic of Non-Inverting op-amp configuration. Schematic courtesy of a Texas Instruments guide for gain design using op-amps.

The following equations\(^\text{10}\) can calculate the desired gain, offset, and the value for the resistors:

\[
\begin{align*}
m & = \frac{V_{out\, high} - V_{out\, low}}{V_{in\, high} - V_{in\, low}} \\
b & = V_{out\, low} - mV_{in\, low} \\
R_2 & = \frac{V_{ref}R_1m}{b} \\
R_g & = \frac{R_2R_f}{m(R_1+R_2)-R_2} \\
\end{align*}
\]

$R_1$ and $R_f$ are used as current limiting resistors for their respective inputs and were chosen to be 10 kΩ, while the voltages represented the input and output range desired:

\[
\begin{align*}
V_{ref} & = 3.3 \text{ V} \\
V_{in\, high} & = 5 \text{ V} \\
V_{in\, low} & = -5 \text{ V} \\
V_{out\, high} & = 3.3 \text{ V} \\
V_{out\, low} & = 0 \text{ V} \\
\end{align*}
\]

However, in following these equations, the value for $R_g$ came to be negative. This was unexpected. Unclear with what the impact of negative resistance would have on this design, SPICE simulations were run for this op-amp configuration using positive resistor values. The results of the simulations indicated that as $R_g$ approaches infinity, $V_{out\, high}$ approaches 4 V. With this in mind, $R_g$ was chosen to be 100 kΩ. Figure 3 demonstrates the resulting linear mapping using the following values for the resistors:

\[
\begin{align*}
R_1 & = 10 \text{ kΩ} \\
R_2 & = 6.6 \text{ kΩ} \\
R_f & = 10 \text{ kΩ} \\
R_g & = 100 \text{ kΩ} \\
\end{align*}
\]
ADC

Considering the nature of the expected CV signals, Texas Instrument’s ADC121S021 12-bit Analog-to-Digital Converter (ADC) was chosen for the job of digitizing the input signals. The operational sampling frequency of the ADC ranges between 50 kHz to 200 kHz, which is more than enough for capturing precise changes to the input signals.

I²C to SPI Bridge

An I²C to SPI bridge is used to translate between the protocols in order to establish communication between the SHARC processor and the ADC. The NXP Semiconductors SC18IS602B is used as an I²C slave and SPI master bridge. This chip will receive control and clock information from the SHARC processor regarding the initialization of the ADC as well as Select address information for the 4:1 Mux. The bridge will then transmit the information using the SPI protocol to the corresponding devices, namely the ADC and Mux. The ADC, in return, will feed the digitized CV data to the bridge, which will be translated to I²C and sent back to the SHARC processor.
Circuit Schematic
Future Work

For future designs, I would like to expand the input voltage range by either introducing a selectable DC offset switch or adjustable voltage bias for the op-amp, design a faceplate for the module, and code a generic user interface for the SHARC processor.
References

2. http://www.doepfer.de/home_e.htm
4. http://www.doepfer.de/home_e.htm
7. https://www.i2c-bus.org/twi-bus/
8. http://i2c.info/