Exams

This course uses the College of Engineering Computer-Based Testing Facility (CBTF) for its quizzes and exams: https://cbtf.engr.illinois.edu.

The policies of the CBTF are the policies of this course, and academic integrity infractions related to the CBTF are infractions in this course.

If you have accommodations identified by the Division of Rehabilitation-Education Services (DRES) for exams, please take your Letter of Accommodation (LOA) to the CBTF proctors in person before you make your first exam reservation. The proctors will advise you as to whether the CBTF provides your accommodations or whether you will need to make other arrangements with your instructor.

Any problem with testing in the CBTF must be reported to CBTF staff at the time the problem occurs. If you do not inform a proctor of a problem during the test then you forfeit all rights to redress.

The testing facility is in 57 Grainger Library, in the basement on the east side of the building.

To resolve any exam or scheduling problems (with technology, or missed appointments, broken exams, etc.), student must communicate with proctors in the CBTF as it happens. The proctors will fix the problem or escalate to the course staff as needed.

You will have 50 minutes to complete each CBTF midterm exam. You should access your exams only during your registered time slot.

Examples of all computer-based exams are available on the CS 233 PrairieLearn. (Exam structure is subject to change.)

Exam 1: Combinational Design

- Computerized Exam
- Covers through Lecture 6 and computing delay
- Format:
  - Short answer questions from PrairieLearn Homeworks
  - NO second chance available
  - 1 Verilog combinational design problem
  - Second chance available
- First chance exam period: Sept. 17 - Sept. 19
- Second chance exam period: Sept. 24 - Sept. 26

Exam 2: Sequential Design

- Computerized Exam
- Format: 1 finite state machine (FSM) design problem
- Second chance available
- First chance exam period: Oct. 1 - Oct. 3
- Second chance exam period: Oct. 8 - Oct. 10

Exam 3: Processor Datapath Design

- Computerized Exam
- Format: 1 Verilog MIPS datapath extension implementation problem
- Second chance available
- First chance exam period: Oct. 15 - Oct. 17

Exam 4: MIPS fundamentals
Computerized Exam
Second chance available
Format:
- Short answer questions about MIPS (example questions and solutions)
  - Includes but is not limited to: calling conventions, interrupts/IO, machine language, pointers, structures/padding, pseudoinstructions, compiling/linking/loading, memory images, RISC vs. CISC, instruction set architectures (ISAs).
  - NO second chance available
- 1 basic MIPS implementation problem
  - Includes many but not necessarily all of the following: function arguments, loops, conditionals, arrays, array indexing, return values, at most a single function call, storing to memory
  - Second chance available
- First chance exam period: Oct. 29 - Oct. 31
  - Second chance exam period: Nov. 5 - Nov. 7

Exam 5: MIPS

Computerized Exam
Format: 1 MIPS implementation problem
- Includes any of the features of Q4 questions plus many but not necessarily all of the following: structures, pointers, arrays of pointers, recursion, function calls inside of loops, storing into a structure/through a pointer, pointer arithmetic
  - Second chance available
- First chance exam period: Nov. 12 - Nov. 14
  - Second chance exam period: Nov. 27 - Nov. 30

Exam 6: Pipelining, Cache Analysis, and Cache Conscious Programming (long form questions)

Written Exam
Format:
- Q1 (Pipelining): true data dependences, structural/data/control dependences, implementing pipelining, forwarding, stalling, branch prediction
  - Second chance available
- Q2 (Cache Analysis): temporal/spatial locality, hit/miss, compute address streams from code, compute miss rate from address stream, tag/index/block offset, direct mapped/set associative/fully associative, write back/write through, write allocate, valid/dirty
  - Second chance available
- Q3 (Cache Conscious Programming): loop inversion, loop fusion, loop fission, tiling (what problems they solve and implementing them), prefetching
  - Second chance available
- First chance exam 6: Dec. 4, 7:00-9:00 pm (Exam rooms: 1404 Siebel Center, 1320 Digital Computing Lab, 100 Materials Science and Engineering Building, and 151 Loomis Lab)
- Second chance exam 6: To be assigned by campus by October 6.
  - One handwritten 8.5" x 11" "cheatsheet" of notes is allowed; you can write on both sides, but you need to leave it with us. No calculators or other electronics are allowed.
    - Cheatsheets cannot be printed in any way. Photocopies are banned. Cheatsheets written on devices (i.e. tablets) and then printed are banned.
- Example past exams
  - Fall 2012: 3rd mid-term (solution)
    3rd mid-term 2nd chance (solution)
  - Spring 2015: Exam6 (solution) Conflict Exam6 (solution)
  - Fall 2016: Exam6 (solution)

Exam 7: Pipelining, Cache Analysis, and Cache Conscious Programming (short answer questions)

Computerized Exam
Format: short answer questions
- NO second chance available
- Performance: latency vs. bandwidth, speedup, CPU iron law, CPI, computing clock cycle time
- Virtual Memory: what problems does it solve?, indirectness, virtual/physical page number, page size, translation lookaside buffer, page fault
- See PrairieLearn for sample exams
- Exam 7 period: Dec. 10 - Dec. 12

Final Exam: Cumulative, including topics introduced after Exam 7 (short answer questions)
• Computerized Exam
• Format: short answer questions
  • NO second chance available
• Cumulative, including all topics from the course
• Some emphasis on topics introduced after Exam 7 such as cache coherence, SIMD, and multicore
• Final exam period: TBA