ECE 385 - Digital Systems Laboratory

Instructors:

For many years, Prof. Janak Patel taught the lecture section. In fall 2009, Prof. Rakesh Kumar taught the lecture section. In Spring 2015, the lecture section is being taught by graduate T.A.s. In any case, you will interact more with TAs for the duration of the class, which is mostly laboratory work.

Prerequisites:

You must take ECE 220 before ECE 385. The wiring skills learned in ECE 110 labs are extremely useful for the first few labs, which are TTL-chip based. An understanding of the concepts presented in ECE 120 is essential to completing the labs in this course. Being able to recall memory, counter, state diagram, and LC-3 concepts is crucial to comprehension of the presented material. A good foundation in C-programming from ECE 220 is important for labs 7-9.

When to Take It:

Many students take ECE 385 in the second semester of sophomore year and the first semester of junior year. It is strongly recommended to take this course as soon as the student has finished ECE 220 so that the material from ECE 120 and 220 will still be fresh. Although some EE students take ECE 385 in their last semester because it is the last required CompE course for EE majors, this is not recommended for students doing well in ECE 120 and 220. Not taking this class will not affect EE curriculum severely, but VHDL/SystemVerilog proficiency of RTL coding, testbench design, and knowledge of FPGAs is a very desirable skill for getting internships in RTL design and verification.

Class Content:

The purpose of the course is to get experience constructing circuits, instead of only working with theoretical design. Each week is a new lab and, unlike other lab courses, much of the work designing and constructing the lab is done outside of class. The lab time itself is usually used for demonstration of your work or debugging if something goes wrong. For the first month you will use TTL ICs and wires to build shift-register computation circuits on a breadboard. The 4th lab switches to SystemVerilog design to be implemented on an FPGA, using Quartus software and programming onto an Altera DE2-115 board. SystemVerilog is a unique language as the code you write is compiled into instructions that the FPGA uses to rewire its hardware—you aren't writing code that is executed on set hardware, you are writing code that creates hardware to perform a function. It is like a virtual simulation of hardware on a computer. It is a good language to know for interviews as SystemVerilog and it's counterpart VHDL can be used to simulate complicated circuits, so employers value your exposure to the language. The SystemVerilog labs progress from fast adder designs, binary multipliers, a working LC-3 you write for the FPGA, and later moving to creating a VGA interface and USB handler to a computer. The 7th lab also introduces C-programming to be used within an Eclipse IDE within Quartus. The class as a whole is good to take as it introduces you to some of the difficulties encountered in actually building physical circuits, as opposed to simply making a theoretical design. Some people also refer to this course as a debugging course, since you learn almost as much about debugging as you do about circuit design. For the last month of the class you will be working on a custom final project involving building a system with RTL on an FPGA; past students have done stuff ranging from video game levels from Super Mario to writing hardware interfaces for peripheral devices on the DE2 board. Other than just documentation and tips about the labs, in class you will learn about using the object-oriented features of SystemVerilog for verification, firmware and RTL design techniques, and an introduction to universal verification methodology (UVM).

Work:

Don't be fooled by the fact that ECE 385 is a 3 hour class. The class requires extensive work each week completing the labs, often taking 10 to 20 hours. Overall, ECE 385 requires much larger weekly time commitment than an average ECE course. Past students said they have spent between 15.3 and 20.7 hours per week on this course. It is extremely helpful to know a lab partner whom you can work with before registering for the class, since properly splitting work and meeting to work on the labs can greatly reduce the time to get the labs working. There are nine labs total and a final project. Not only does the designing and wiring have to be completed outside of class, but students should also debug before demonstrating their lab. Additionally, the labs require reports which will take several hours to complete. Sometimes it helps to ask a TA about grading criteria. You will spend more time on the labs as the semester progresses and the difficulty of the labs increases. You will get several weeks to work on the final project; make sure you start early in case you run into difficulties. It is possible to take this class with other work intensive classes, but you will have a heavy semester. This is a challenging course, but finishing it will be rewarding especially if you wish to go into RTL and chip design.

Life After:

Computer engineers thrilled by this course should take ECE 391 right away, which is a prerequisite for ECE 411, the next course using SystemVerilog. SystemVerilog is in a family of Hardware Description Languages (HDLs) including VHDL, Verilog, and SystemC. HDLs are similar to programming languages in that once you've learned one, the similarities of concepts between HDLs overwhelm the differences of syntax. Learning SystemVerilog in 385 prepares you well to use any HDL in the workplace. There is a huge job market for working with FPGAs. Additionally, the concepts learned in this class are applicable to ASICs and processors. The "Life After" section for ECE 411 elaborates on career opportunities.