Instructors:

Professor Sarita Adve has apparently taught this course for a long time. Among other accomplishments, she co-developed the memory models for the C++ and Java programming languages.

Prerequisites:

CS 232, Computer Architecture II, is listed as the only prerequisite. ECE 391 Computer Systems Engineering should be sufficient as the material CS 433 covers is very similar to that of ECE 411 Computer Organization and Design. Basic pipelining knowledge and cache coherency should be briefly studied before taking the course when coming from ECE 391.

When to Take It:

CS 433 should be taken after ECE 391 and within a semester before or after ECE 411. If taken prior to ECE 411, students should be able to focus more on the lab component of ECE 411, since they would already have the theory. If CS 433 is taken after ECE 411, students should be able to obtain an easy A.

Class Content:

Very similar to ECE 411, this course covers various topics in processor optimization. Knowledge of the basic 5-stage pipeline is assumed, then expanded to include multiple execution units, pipelined execution units and data forwarding between stages among other basic techniques. The full list of topics, referenced from the course website, is listed below. A major drive of the course is reordering instructions so that each clock cycle is utilized most efficiently while slower instructions cause delays. Presentations are given at the end by graduate students in the course that tie topics learned into modern-day CPUs and GPUs.

- Introduction – review of fundamental performance issues, power and reliability, cost vs. price, basic pipeline structure
- Instruction level parallelism – hardware and software techniques (e.g., dynamic scheduling, superscalar, static and dynamic branch prediction, VLIW, loop unrolling)
- Memory hierarchy – advanced concepts in caches (e.g., prefetching, lockup-free caches, and multi-level caches), main memory, and virtual memory.
- Multiprocessors/multicore – overview of different models, cache coherence with shared-memory systems/multicore (snoopy and directory solutions), synchronization, memory consistency models.
- Data parallel architectures – vectors, SIMD, GPUs – depending on available time
- Storage systems, I/O – depending on available time
- Recent advances in architecture and future challenges – depending on available time

Almost the entire class is covered, with more or less detail on most topics, in this YouTube video.

Work:

There are 7-8 homework assignments each semester, depending on how quickly material is covered in class, and each should take 3-5 hours. All information required for the homework is available from lecture; the book isn’t necessary. As long as students attend lectures and do the homework, only a moderate review should be necessary before the midterm and non-cumulative final.

Life After:

This class has no benefits over ECE 411 unless a student is an EE and wants the knowledge of ECE 411 but not the lab component. A good number of graduate students tend to take the class, likely continuing on to CS 533, also taught by Professor Adve.